

# Operation Region Selector Circuit to Obtain Maximum Efficiency of 250 W Boost Converter

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**Abstract**—Interleaved boost converter gives good conversion efficiency due to its zero-current switching capability when operating in discontinuous conduction mode while keeping its input-output ripple current low. However, operating this kind of converter at interleaved operation for all the time gives poor efficiency under light-load condition. In this paper, an automatic operation region selector switch based on detection of the continuous or discontinuous current mode is proposed. With this switch, during the light-load condition, only one converter is activated, while during full-load condition both converters will be activated. The simulation results using LTSpice software show that the proposed boost converter has a better efficiency compared to the conventional boost converter with efficiency range of 84.6 % to 95.32 % under various load conditions.

**Kata Kunci**—Boost converter, Efficiency, LTSpice.

## I. INTRODUCTION

Boost converter or step-up converter is used to convert a certain dc level voltage to a higher level dc voltage with a few amount of ac ripples (quasi-dc voltage) [1], [2]. In power conversion, particularly renewable energy, the boost converter is an important device as power electronics interface to provide a regulated output voltage to meet the load requirements because, generally, renewable energy sources have quite low and unregulated output voltage [3], [4]. As a switch mode power supply (SMPS), boost converter operation based on switching principle driven by pulse width modulation (PWM) with a constant frequency. Based on the amount of energy that is delivered to the load during each switching period, boost converter operates in two different modes, known as continuous conduction mode (CCM) and discontinuous conduction mode (DCM) [5], [6].

The inductor current in continuous mode (CCM) is always greater than zero, so the average current of the inductor is always greater than half the peak value of the inductor current ripple ( $\Delta I_{L, peak}$ ), as shown in the following equation [7].

$$I_{L(avrg)} > \frac{\Delta I_{L(Peak)}}{2} \quad (1)$$

In discontinuous mode (DCM), the inductor current falls to zero before completion of the switching period, so the energy stored in the inductor will be wholly transferred to the load before completing a switching period [8].

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To obtain a better energy transfer, the basic topology of the boost converter is developed into an interleaved boost converter by doubling the power components, such as the inductor, electronic switch, and diode. An interleaved boost converter is driven by multiple PWM with a certain phase difference depending on the number of interleaved phases (N). The main advantages of the interleaved boost converter are lower current and voltage ripple, thereby reducing the filter size. Interleaved boost converter that operates at light-load or in the range between 20% to 40% of maximum power, the inductor current becomes smaller due to the doubling of the inductor number, thus forcing the converter to operate in a discontinuous conduction mode. Interleaved boost converter operating in DCM mode will cause large peak currents and high current stress causing losses in power components that lead to poor efficiency [9].

This paper presents design and analysis of 250 W boost converter that combined with an automatic operation region selector switch in the form of interleaved and non-interleaved operation region selector circuit to avoid discontinuous conduction mode when operating under light-load condition or 20% to 40% of maximum power.

## II. MODEL AND DESIGN

The models and design are done using LTSpice software with technical specification as shown in Table I.

TABLE I  
SYSTEM PARAMETERS AND SPECIFICATIONS

Parameter	Specification
Maksimum Power ( $P_{max}$ )	250 W
Input Voltage ( $V_{in}$ )	32.48 V <sub>dc</sub> - 34.94 V <sub>dc</sub>
Output Voltage ( $V_O$ )	120 V <sub>dc</sub>
Output Voltage ripple ( $\Delta V_O$ )	< 1%
Input Current ( $I_{in}$ )	7.71 A
Output Current ( $I_O$ )	2.08 A
Switching Frequency ( $f_s$ )	100 kHz
Duty Cycle ( $D$ )	0.71 - 0.73

The designing flow consists of the design of the converter, PWM control settings and the design of the operating region selector circuit which is then integrated into one system. The design steps are described as follows.

### A. Converter Design

1) *Inductor Selection*: Inductor selection based on the inductor minimum value and inductor saturation current. The inductor minimum value refers to the maximum duty cycle ( $D_{max}$ ) of 0.73, the inductor current ripple ( $\Delta I_L$ ) of 1.54 A, the minimum input voltage ( $V_{in,min}$ ) of 32.48 V and 100 kHz

switching frequency ( $f_s$ ). Since in this study two interleaved phases ( $N=2$ ) which consist of two inductors are used, then the minimum size of the inductor ( $L_{1,2}$ ), in order to operate in CCM, can be calculated using the following equation.

$$L_{1,2(\min)} = \frac{V_{in,\min} \cdot D_{\max}}{\Delta I_L \cdot N \cdot f_s} = \frac{32.48 \cdot 0.73}{1.54 \cdot 2 \cdot 100000} = 76.98 \mu\text{H} \quad (2)$$

The inductor saturation current depends on input current ( $I_{in}$ ) of 7.71 A, the inductor current ripple ( $\Delta I_L$ ) of 1.54 A and two interleaved phases ( $N=2$ ), then the inductor current saturation value can be calculated by the equation as follows.

$$I_{L,\text{sat}} = I_{in} + \frac{\Delta I_L}{2} = 7.71 + \frac{1.54}{2} = 8.48 \text{ A} \quad (3)$$

Through the calculation of the inductor minimum value in (2) and (3), the inductor used is model of WURTH ELECTRONIK® 74435588200WE-HCI with an inductance of 82  $\mu\text{H}$ , DC resistance of 0.0304  $\Omega$  and saturation current of 8.50 A.

The most significant loss to the inductor are the copper winding loss when the current is flowing (copper loss). The copper loss refers to the current value of ( $I_L$ ) 7.71 A, the resistance in the inductor ( $DC_R$ ) 0.0304  $\Omega$ , and the number of interleaved phases ( $N = 2$ ), so the copper loss on the selected inductor can be calculated using the following equation.

$$\begin{aligned} P_{ind,copper-loss} &= \frac{I_L^2}{N} (DC_{R1} + DC_{R2}) \\ &= \frac{7.71^2}{2} (0.0304 + 0.0304) \\ &= 1.81 \text{ W} \end{aligned} \quad (4)$$

2) *MOSFET Selection*: MOSFET selection refers to the drain-source voltage ( $V_{DS}$ ), the maximum operating capability of drain current ( $I_{D,max}$ ), drain-source on resistance ( $R_{DS(on)}$ ), and also considering the parasitic elements that cause switching losses and gate charging losses [10]. The maximum operating voltage of the MOSFET should exceed the nominal output voltage ( $V_O$ ), while the maximum operating capability of the drain current ( $I_{D,max}$ ) refers to the maximum duty cycle value ( $D_{Max}$ ) 0.73, the current ripple ( $\Delta I_L$ ) of 1.54 A, the output current ( $I_O$ ) of 2.083 A, therefore,  $I_{D,max}$  can be calculated using the following equation.

$$I_{D,\max} = \frac{\Delta I_L}{2} + \frac{I_O}{1 - D_{Max}} = \frac{1.54}{2} + \frac{2.083}{1 - 0.73} = 8.48 \text{ A} \quad (5)$$

From (5), as well as adding a 60% safety margin, the MOSFET used is a model of N-Chanel BSC900N20NS3 MOSFET with 200 V drain-source ( $V_{DS}$ ), 15 A drain current ( $I_D$ ), and 0.09  $\Omega$  on resistance ( $R_{DS(on)}$ ). Losses in the selected MOSFET consist of conduction loss, switching loss, and gate loss.

The conduction loss in the MOSFET refers to drain current ( $I_d$ ) of 7.71 A, ON resistance, maximum duty cycle ( $D_{max}$ ),

and the number of interleaved phases ( $N = 2$ ), hence the conduction losses in the selected MOSFET can be determined as follows.

$$\begin{aligned} P_{Sw,cond-loss} &= N \cdot R_{DS(on)} \cdot D_{\max} \left( \frac{I_{in}}{N} \right)^2 \\ &= 0.09 \cdot 0.73 (7.71)^2 = 3.91 \text{ W} \end{aligned} \quad (6)$$

The switching loss in the MOSFET refers to the output voltage ( $V_O$ ) of 120 V, peak current ( $I_{D,peak}$ ) of 8.48 A, ON overlapping time ( $t_{on}$ ) 9.68 ps, and OFF overlapping time ( $t_{off}$ ) 4.75 ps, thus, the switching loss in the selected MOSFET can be calculated as follows.

$$\begin{aligned} P_{Sw,sw-loss} &= N \cdot \frac{1}{2} \cdot \frac{I_{in}}{N} (t_{on} + t_{off}) f_s \\ &= \frac{1}{2} \cdot 120 \cdot 7.71 [(9.68 + 4.75) 10^{-9}] 100000 \\ &= 0.67 \text{ W} \end{aligned} \quad (7)$$

The gate charge loss is affected by the gate voltage ( $V_G$ ) of 7.2 V, and the total gate charge ( $Q_g$ ) of 11.6 nC and switching frequency ( $f_s$ ) of 100 kHz, therefore the gate charge loss ( $P_{Sw,gate-loss}$ ) calculated as follows.

$$\begin{aligned} P_{Sw,gate-loss} &= 2 \cdot V_G \cdot Q_G \cdot f_s \\ &= 2 \cdot 7.2 \cdot (116 \cdot 10^{-10}) 100000 \\ &= 0.02 \text{ W} \end{aligned} \quad (8)$$

3) *Diode Selection*: Determination of the output diode on the boost converter based on current and voltage rating, diodes with forward and reverse currents are greater than the output voltage ( $V_O$ ) and output current ( $I_O$ ) is desirable. To minimize losses, diodes that have relatively small reverse ( $t_{rr}$ ), forward ( $V_F$ ), and reverse ( $I_F$ ) currents are used. Diode model used in this research is ultra fast switching diode RFN5BM2S with a time reverse recovery ( $t_{rr}$ ) 25 ns, forward voltage ( $V_F$ ) 0.98 V, forward current ( $I_F$ ) 5 A, reverse voltage ( $V_R$ ) 200 V, and reverse current ( $I_{RM}$ ) 10  $\mu\text{A}$ .

Losses on the selected diode consist of conduction loss ( $P_{D,cond-loss}$ ) and reverse recovery loss ( $P_{D,rr-loss}$ ) which can be calculated as follows.

$$\begin{aligned} P_{D,cond-loss} &= N \cdot V_F \cdot \left( \frac{I_{out}}{N} \right) (1 - D_{\max}) \\ &= 0.98 \cdot 2.083 (1 - 0.73) = 0.55 \text{ W} \end{aligned} \quad (9)$$

$$\begin{aligned} P_{D,rr-loss} &= N \cdot \frac{1}{2} \cdot V_{out} \left( \frac{I_{RM}}{N} \right) t_{rr} \cdot f_s \\ &= \frac{1}{2} \cdot 120 \cdot (10 \cdot 10^{-6}) (25 \cdot 10^{-9}) \cdot 100000 \\ &= 1.5 \cdot 10^{-6} \text{ W} = 1.5 \mu\text{W} \end{aligned} \quad (10)$$

4) *Output and Input Capacitor Selection*: The output capacitor acts as a voltage ripple filter and supplies the load current when the electronic switch is closed ( $t_{on}$ ). If the boost converter operates in interleaved mode with two interleaved

phases ( $N = 2$ ), the frequency at the output side will be twice of the switching frequency, so with the output current ( $I_o$ ) of 2.083 A, the output voltage ( $V_o$ ) of 120V, and the desired output voltage ripple ( $V_r$ ) at 1% of the output voltage, then the output capacitor ( $C_{out}$ ) can be calculated as follows.

$$C_{out} \geq \frac{I_o}{V_r \cdot V_o \cdot n \cdot f_s} \geq \frac{2.083}{1.2 \cdot 120 \cdot 2 \cdot 100000} \geq 0.072 \mu\text{F} \quad (11)$$

From the output capacitor minimum value calculation in (11), the output capacitor is formed from two pieces of 10  $\mu\text{F}$  capacitors connected in parallel to minimize the equivalent series resistor (ESR) with 20  $\mu\text{F}$  total capacitance. The model of capacitor used in the simulation circuit is KEMET® EDH106M200.

Unlike the output capacitor, the use of input capacitor for boost converter is not critical due to the existence of inductor connected in series with the voltage source [11].

### B. PWM Control Settings

LT3758 is used as a PWM controller configured at a constant frequency of 100 kHz. The basic operating arrangements of LT3758 are outlined as follows.

1) *Output Voltage Setting*: To establish the output voltage on the boost converter is done by providing a 1.6 V feedback voltage as reference voltage according to the LT3758 standard [11]. The feedback voltage is obtained from the voltage divider resistor ( $R_{F1}$  and  $R_{F2}$ ). Since the output voltage ( $V_o$ ) 120 V and the  $R_{F2}$  resistance value is set at 100 k $\Omega$ , then  $R_{F1}$  can be calculated using the following equation.

$$\begin{aligned} R_{F1} &= \left( \frac{V_o \cdot R_{F2}}{1.6} \right) - R_{F2} \\ &= \left( \frac{120 \cdot 100000}{1.6} \right) - 100000 = 7.4 \text{ M}\Omega \end{aligned} \quad (12)$$

2) *Determination of  $R_{SENSE}$* :  $R_{SENSE}$  is used to generate the reference current in PWM control. To determine the value of the  $R_{SENSE}$  refers to peak current ( $I_{D,Peak}$ ) of 8.48 A and peak voltage ( $V_{SENSE}$ ) of 0.08 V, hence the  $R_{SENSE}$  can be calculated by the following calculation.

$$R_{SENSE} = \frac{V_{SENSE}}{I_{D,peak}} = \frac{0.08}{8.48} = 9.43 \text{ m}\Omega \quad (13)$$

3) *SHDN/UVLO Setting*: SHDN/UVLO is the enable pin that is used to activate the LT3758 chip and as a protection when undervoltage and overvoltage occur by providing a reference voltage of 1.22 V [11]. The reference voltage is formed from the voltage divider resistor network ( $R_1$  and  $R_2$ ), if  $R_2$  is determined at 47 k $\Omega$  with the minimum input voltage ( $V_{in,min}$ ) 32.48 V, hence the value of  $R_1$  can be calculated using the following equation.

$$\begin{aligned} R_1 &= \left( \frac{V_{in,min} \cdot R_2}{1.22} \right) - R_2 \\ &= \left( \frac{32.48 \cdot 47000}{1.22} \right) - 47000 = 1.2 \text{ M}\Omega \end{aligned} \quad (14)$$

### C. Operating Region Selector Circuit Design

The proposed boost converter is designed in the interleaved operating region with continuous conduction mode (CCM), driven by two LT3758 IC's to generate PWM 1 and PWM 2 signals that are phase delayed by 180°. When the boost converter operates at 20 to 40% of the maximum power, the PWM 2 signal will be disabled by supplying 0 V to the SHDN/UVLO pin. When one of the PWM's is inactive, one of the two inductors will not behave, so the current from the source will flow completely through one inductor only, thus causing the boost converter initially operating interleaved become non-interleaved. To carry out the concept of control, an electronic circuit is designed to detect the inductor current conduction mode under various load conditions in order to select the interleaved and non-interleaved operating region with respect to the inductor current characteristic equation that shown in (1), thereby an operating configuration can be obtained, as shown in Table II.

TABLE II  
OPERATING CONFIGURATION OF PROPOSED BOOST CONVERTER

Inductor Current Characteristic	Conduction Mode	PWM 1	PWM 2	Operating Region
$I_L > \frac{\Delta I_{L(Peak)}}{2}$	CCM	On	On	Interleaved
$I_L < \frac{\Delta I_{L(Peak)}}{2}$	DCM	On	Off	Non-Interleaved

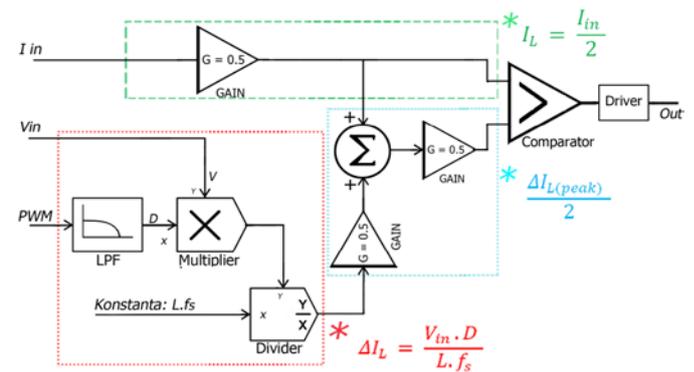


Fig. 1 The block diagram of operating region selector.

The output of the operating area selector circuit is a voltage used as SHDN/UVLO trigger on one of the PWM controller unit, the voltage obtained from the comparison between half the peak value of the inductor current ripple ( $1/2\Delta I_{L(peak)}$ ) with the average inductor current ( $I_{L(average)}$ ) through the role of the comparator. The inductor current variable is obtained from the input current sensor which is then converted to the voltage form, whereas for the peak value of the inductor current ripple is obtained from the operation of the mathematical equations applied into the block diagram as shown in Fig. 1.

In the block diagram, the current sensor using LT6105, the multiplier uses AD633, as the operator used low-power Op-Amp LM358 configured as the low-pass filter, divider, summing amplifier and comparator.

III. RESULTS AND DISCUSSION

Simulations are performed to verify the performance of boost converter combined with interleaved and non-interleaved operation regions selector circuit that has been designed in various load conditions. The system was tested based on SPICE simulation using LTspice software with the arrangement as shown in Fig. 2.

Fig. 3 shows the simulation results of the converter output voltage under various load conditions, where the output voltage remains in the range of 120.3 V despite a load change. It showed the success of the LT3758 as a PWM controller as well as the voltage compensator. It can be seen from Fig. 3

that ripple output voltage is less than 1% of the nominal output voltage. This happens because of the existence of output capacitor as a filter.

Fig. 4 shows the input and output voltage of the comparator with varying load power from 10 W to 250 W.

When the converter operates at a power of 100 W to 250 W (more than 40% of maximum power), the voltage representing the average current of the inductor  $V(I_L)$  always greater than half the peak of inductor current ripple  $V(1/2dI_{L, peak})$ , then the comparator output voltage of 6.92 V is generated to trigger both PWM controllers, so the boost converter operates on interleaved region, as shown in Fig. 5.

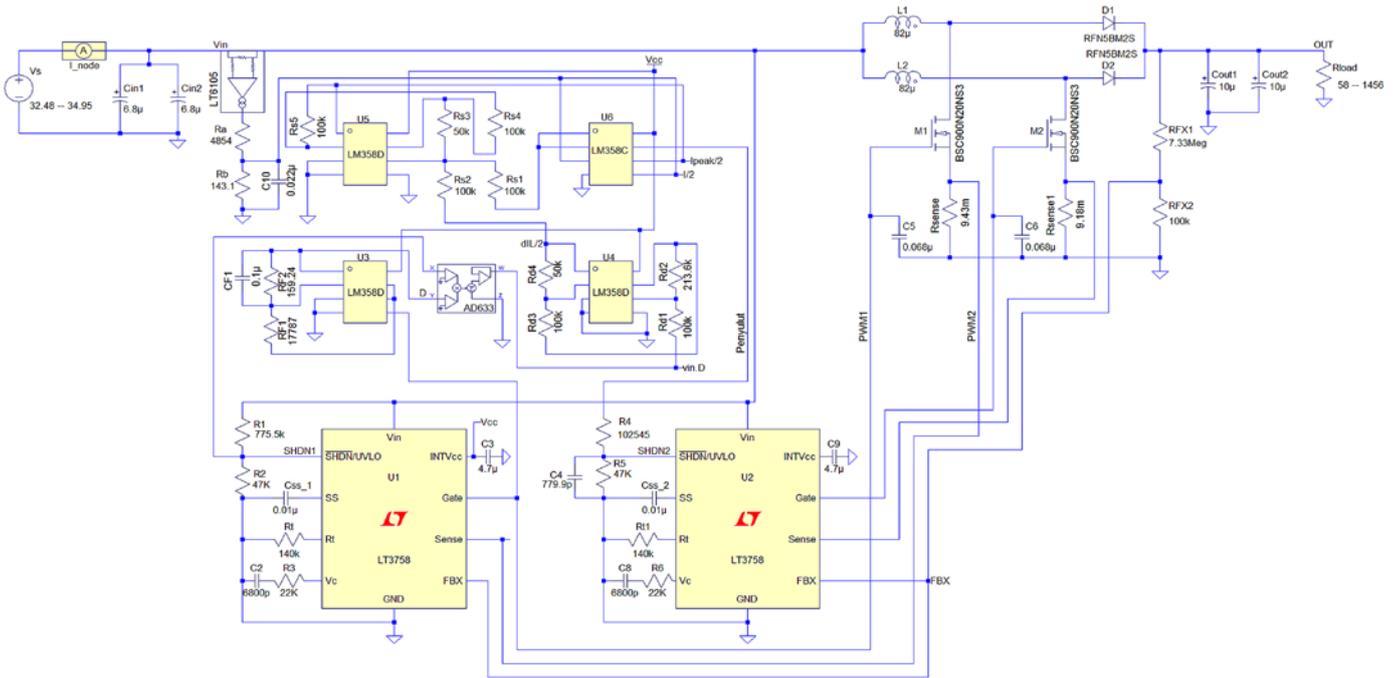


Fig. 2 Simulation circuit arrangement in LTspice.

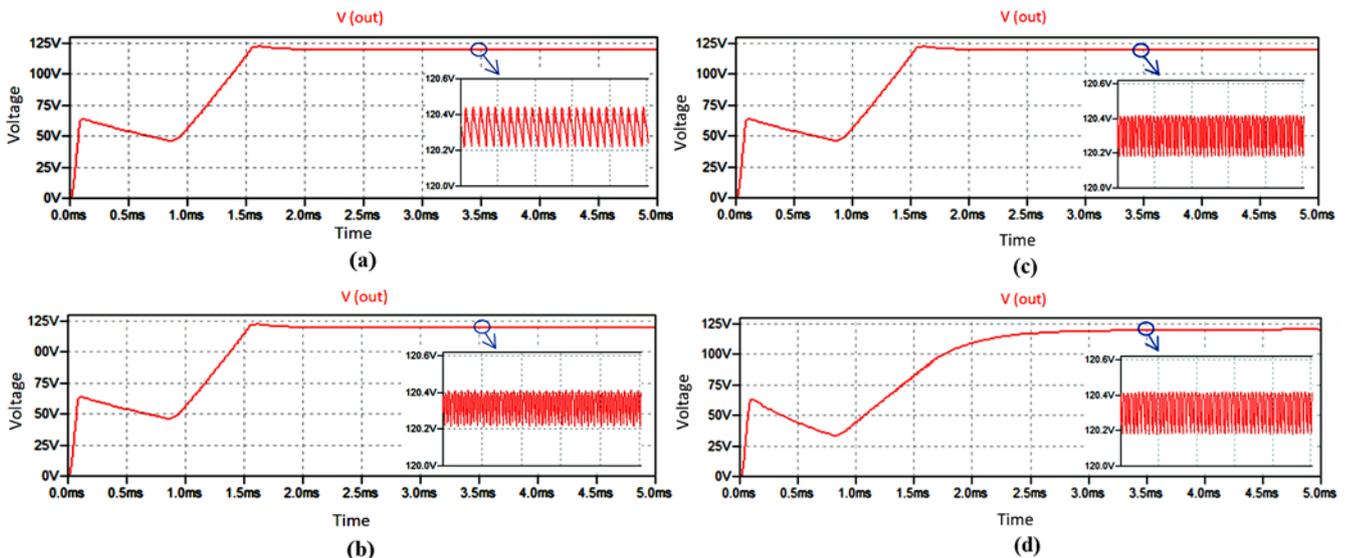


Fig. 3 Converter output voltage under various load conditions, (a) 25% load, (b) 50% load, (c) 75% load, (d) 100% load.

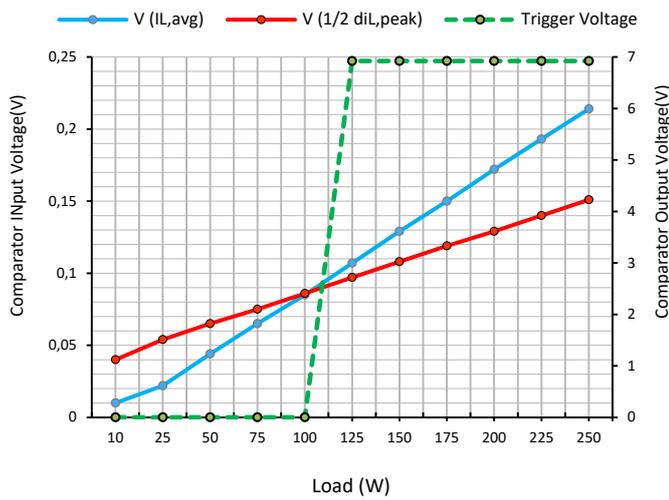


Fig. 4 Comparator input and output voltage under various load conditions.

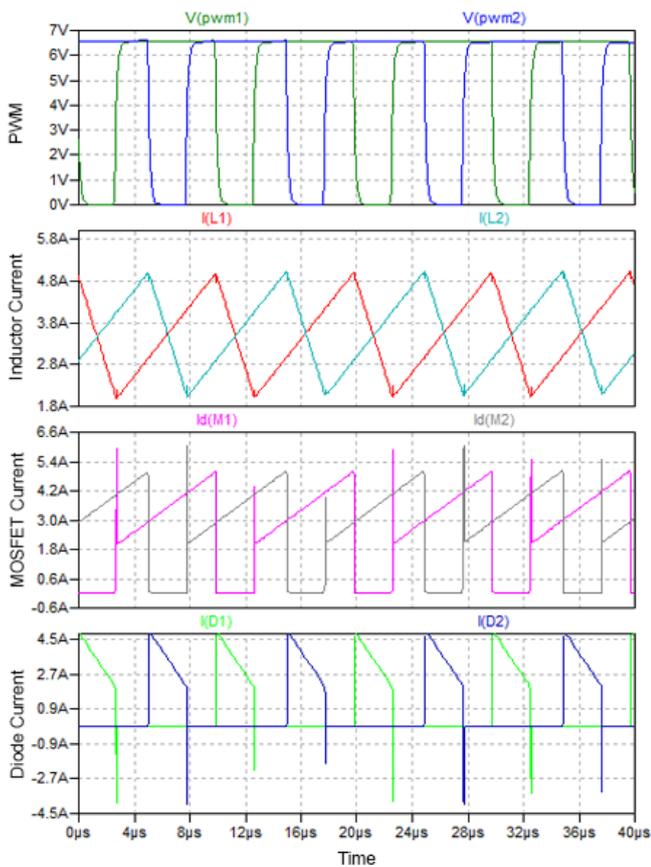


Fig. 5 Interleaved waveform.

When the converter operates at a power of 10 W to 100 W (less than 40% of maximum power), the voltage representing the current inductor current  $V(I_L)$  is less than than half the peak of inductor inductor current ripple  $V(1/2dI_L, peak)$ , so the comparator output voltage becomes 0 V and disables the SHDN/UVLO pin and one of the PWM signals becomes inactive, so the boost converter operates on non-interleaved region, as shown in Fig. 6.

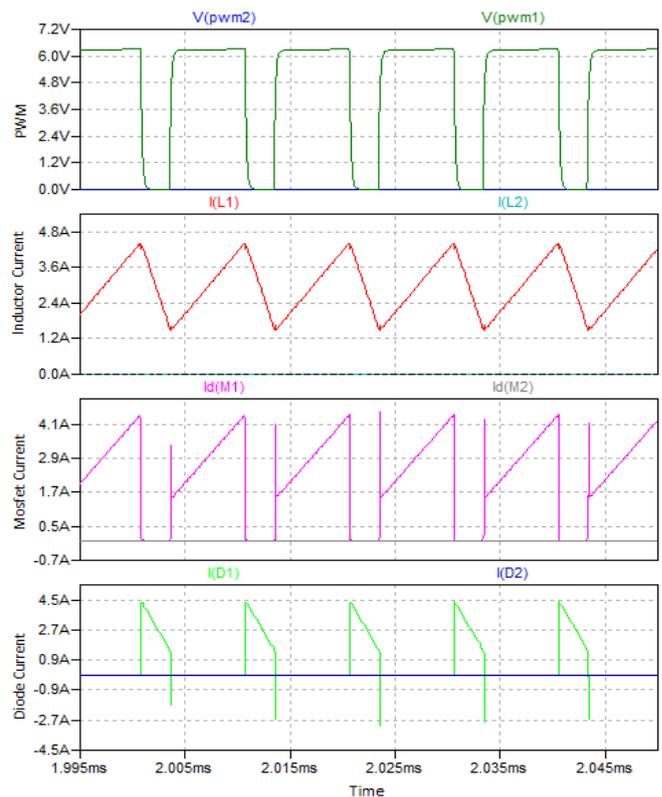


Fig. 6 Non-interleaved waveform.

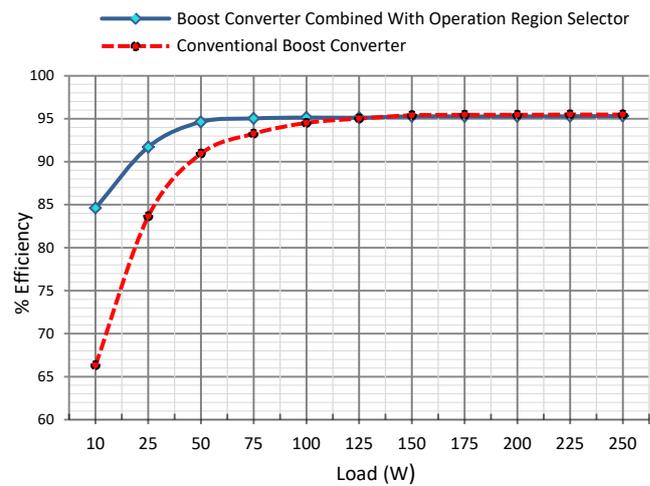


Fig. 7 Efficiency comparison.

Fig. 7 shows the efficiency comparison of the interleaved boost converter combined with the operation region selector circuit and the conventional boost converter.

When operating at full-load conditions (100 W to 250 W), the boost converter combined with operation region selector circuit yields an efficiency of 95.32%, while the conventional boost converter circuit yields an efficiency of 95.48%. Conversely, when operating under light-load conditions (10 W to 100 W), the conventional boost converter yields an efficiency of 66.31%, while the boost converter combined with operation region selector circuit yields an efficiency of 84.6 %.

## IV. CONCLUSION

Design and analysis of 250 W boost converter that combined with an automatic operation region switch in the form of interleaved and non-interleaved operation region selector circuit has been done using LTspice software. The simulation results show the output voltage is in the range of 120.3 V, with less than 1% output voltage ripple at each load condition. The boost converter combined with the operation area selector circuit obtains better efficiency compared to conventional boost converter with an efficiency above 80% which ranges from 84.6% to 95.32%, resulting in a better operating range with maximum conversion efficiency.

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## REFERENCES

- [1] J. Wang, "Design of a Boost DC-DC Converter for Energy Harvesting Applications in 40nm CMOS Process," M.Sc. thesis, Delft University of Technology, Delft, Netherlands, 2014.
- [2] S. Mohd, A. A. Rahim, N. Mazalan, and S. Y. Xia, "Design of DC-DC Boost Converter with LTSPICE Simulation Software," *Multi-Disciplinary Res. J.*, Vol. 1, No. 2, pp. 20–27, 2016.
- [3] N. Coruh, S. Urgan, T. Erfidan, and S. Ozturk, "A Simple And Efficient Implementation Of Interleaved Boost Converter," *6th IEEE Conference on Industrial Electronics and Applications*, 2011, pp. 2364–2368.
- [4] N. Singh and S. P. Phulambrikar, "Design and Analysis of an Efficient Boost Converter for Renewable Energy Sources," *IJSRP*, Vol. 5, No. 1, pp. 1–6, 2015.
- [5] M. Kamil, "AN1114: Switch Mode Power Supply (SMPS) Topologies (Part I)," Microchip Technology, Application Note, pp. 1–48, 2007.
- [6] N. Mohan, Tore M. Undelan, and W. P. Robbins, *Power Electronics: Converters, Applications, and Design*, 2nd ed., New York, USA: John Wiley & Sons, Inc., 1994.
- [7] B. C. Barry, J. G. Hayes, M. G. Egan, M. S. Rył, J. W. Masłoń, and K. J. Hartnett, "CCM and DCM Operation of the Integrated- Magnetic Interleaved Two-phase Boost Converter," *2014 Twenty-Ninth Annual IEEE Applied Power Electronics Conference and Exposition (APEC)*, 2014, pp. 35–42.
- [8] M. H. Rashid, *Power Electronics Handbook*, San Diego, CA, USA: Academic Press, 2001.
- [9] S. E. Babaa, "Novel Switch Adaptive Control to Improve the Efficiency of Boost Converter in Photovoltaic Systems," *J. Power Energy Eng.*, Vol. 5, No. 7, pp. 1–14, 2017.
- [10] S. Abdel-Rahman, "CCM PFC Boost Converter Design," Infineon Technologies North America, Design Note, 2013.
- [11] "LT3758/LT3758A datasheet," Linear Technology, Milpitas, CA, USA.